Locking a Frequency with 555

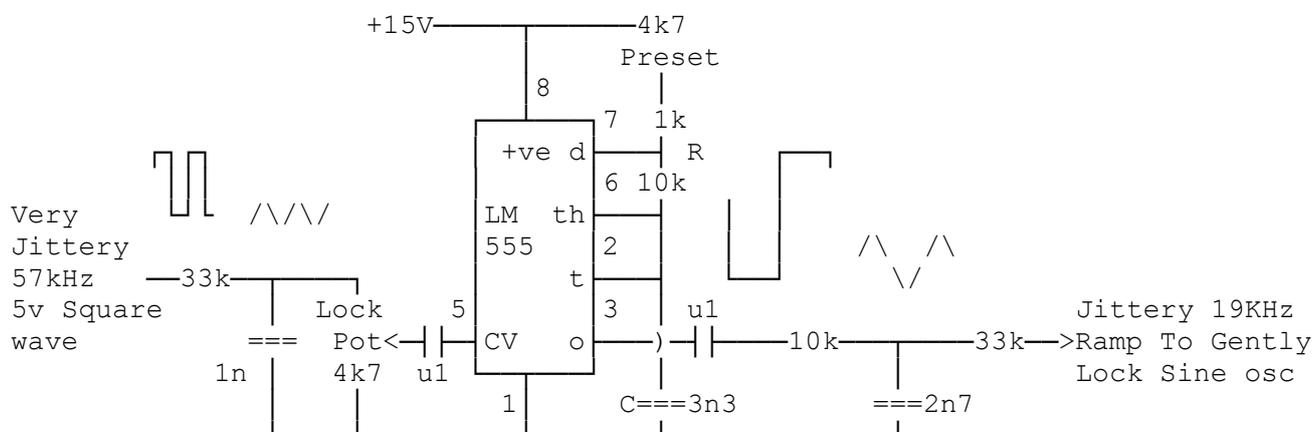By G8MNY   (Updated Jan 16)
(8 Bit ASCII graphics use code page 437 or 850, Terminal Font)

Year ago I had a valve B&W 405 line camera that used many double triode
astables to lock the 50Hz frame timebase to line interlaced 11250Hz line
frequency! I reworked it for 625 line by raising the 2x line LC osc to 31250Hz
& locking 4x 1/5 the frequency astables to it (>6250>1250>250>50Hz) to
correctly lock the interlaced frame timebase.

The other day I had a similar problem, to lock an old 1980s stereo coder design
to a modern RDS unit. This is normally done the other way around, locking RDS
data unit from the 19kHz pilot! The trouble with my approach was there was no
clean 57kHz to start with! The Pic RDS generator had 6 data bits added to
synthesise the QPSK sine waves etc. So I used the MSB data to give the best
57kHz starting clock.

```
                          +15V─────────────4k7
                           │         │      Preset
                           │         │        │
                           │   8     │        │
                           │         │ 7   1k │
      ┌─┐   ┌─┐          ┌─────────┐ ├─────R──┤
      │ │   │ │          │+ve    d │ │        │     ┌──────┐
Very  │ │   │ │  /\/\/   │         │ │ 6  10k │     │      │
Jittery   └─┘   └─        │LM    th │ ├────────┤     │      │
57kHz ──33k──┐           │         │ │ 2      │     │   /\  /\
5v Square    │   Lock   5│555    t │ ├────────┘     │     \/        Jittery 19KHz
wave         │   Pot<─┤├─┤CV     o │ )─┤├───10k──────33k──>Ramp To Gently
            ===      <  u1│         │ │ u1    │              Lock Sine osc
            1n    4k7    └─────────┘ │        │
                           │   1     │        │
                           │         C===3n3  ===2n7
      ─────────────────────┴─────────┴────────┴──────
```

I found a slightly less jittery lock was obtained when both square waves were
ramped to a triangle with a CR. The 555 19kHz astable is loosely locked to the
57kHz by modulating the Control Voltage rail used to compare the CR voltage.
The smaller the lock input the more loosely locked (higher Q) result, but less
stable to temp/Voltage changes. The C & R components that set the 19kHz need to
be high stability types!

Result, after getting the ramps right & enough lock drive to the 555 astable @
19kHz, it reliably locks up hot & cold, & with Wayne bridge sine osc gives a
stable locked osc in the right phase too in my application!

The above principle can be used for up & down locking of different frequencies
in many fractions etc. e.g. 50Hz from 60Hz.

See tech buls "Off Air Lock for Ref Osc.", & "Simple 1kHz AF Test Osc".

Why don't U send an interesting bul.

73 De John, G8MNY @ GB7CIP